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A LOW POWER SRAM USAGE IN FPGA MEMORY CELL

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KEYWORDS : VLSI, SRAM ,FPGA

ABSTRACT
Low power has emerged as a principal theme in today's electronics industry. With ever increasing level of device integration and the growth in complexity of electronic circuits, increasing the demand of portable electronics devices and also dependence on the battery operated devices motivating the VLSI designers to reduce the power dissipation, of the VLSI circuits. The reduction of power is the most often used measures of the efficiency of VLSI circuits. Low power circuits have long battery life. Power consumption due to memory accesses in a computing system often constitutes the dominant portion of the total power consumption. Measures have to be taken to reduce power consumption in memories. FPGA provide a short time to market and low design cost, which make them increasingly attractive. So a FPGA is designed with various blocks in it.The basic motive of this paper is to analyze the SRAM memory cell which will consume lesser power. FPGA consists of memory block, logical block, switch block, connection block. The memory block consists of memory cell. The memory cell used is 10T SRAM cell. The 10T SRAM cell is designed using c2mos logic which consumes less power. The designed 10T SRAM cell is used in the read circuit of the memory block. The logic block and switch block is also designed. Power results of FPGA blocks have been obtained and power results of existing system and proposed system have been compared. Simulation results show significant improvements in reduction of power consumption. All the simulations have been carried out on 180nm technology at Tanner s-edit tool.

INTRODUCTION
Low voltage circuit has become more and more important because of the increasing demand for low power applications .With ever increasing operating frequency and processing capacity per chip, large currents have to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Battery life in portable electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices.
Besides this there are number of reason, for the motivation of this project work: Shrinking of device size, Growth of Portability, Reliability and Battery size. Every digital system now a days is strongly dependent on the memory we can also say that no digital system now a days can be built without memory. It is also the heart of any microprocessor and that is why most of the research in low power design is going to design the memory. The basic motive of this project work is to analyse the SRAM memory cell which will consume lesser power.
The increasing prominence of portable systems and the need to limit power consumption (and hence, heat dissipation) in very-high density ULSI chips have led to rapid and innovative developments in low-power design during the recent years. The driving forces behind these developments are portable applications requiring low power dissipation and high throughput, such as notebook computers, portable communication devices and personal digital assistants.
In most of these cases, the requirements of low power consumption must be met along with equally demanding goals of high chip density and high throughput. Hence, low-power design of digital integrated circuits has emerged as a very active and rapidly developing field of CMOS design. FPGAs are pre-fabricated silicon devices that can be electrically programmed to become almost any kind of digital circuit or system they have many advantages over ASIC. ASICs are designed for specific application using CAD tools and fabricated at a foundry. Developing an ASIC takes very much time and is expensive. Furthermore, it is not possible to correct errors after fabrication.
In contrast to ASICs, FPGAs are configured after fabrication and they also can be reconfigured. This is done with a HDL which is compiled to a bit stream and downloaded to the FPGA. Due to the increase of transistor density FPGA were getting more powerful over the years. On the other hand the development of ASICs was getting slower and more expensive. Therefore FPGAs are increasingly applied to high performance embedded

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systems.A SRAM is a memory element that is a key part of the core of many systems. Most high performance system has SRAM in them. SRAM consumes less power when compared DRAM. It does not periodically refresh. SRAM is very fast when compared to Dynamic RAM. In this project an FPGA is designed using 10T SRAM cell. Logic block, logic elements is also implemented. The designed blocks power results will be obtained.

EXISTING SYSTEM

FPGA is designed with various blocks such as memory block, logic block and switch block. The memory block consists of read circuit. The read circuit consists of memory cells. The memory cell used is 10T SRAM cell. Shift registers are used in the read circuit of the memory block. The various blocks will be designed and power results will be obtained.

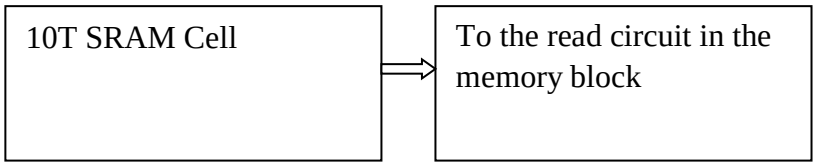

Figure 4.1 10T SRAM cell

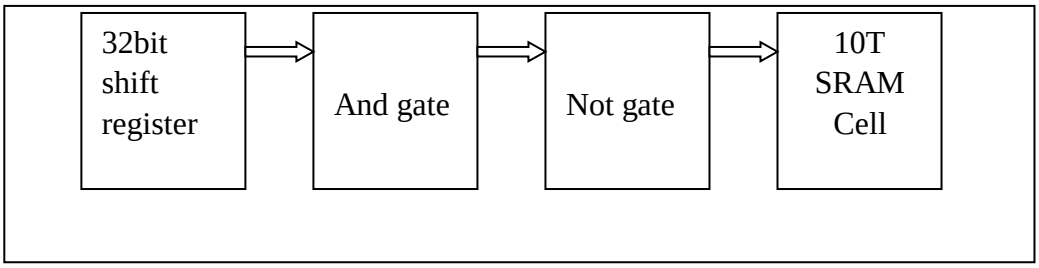

Figure 4.2 Read circuit in the memory block

4.2 PROPOSED SYSTEM

Low power circuit has become more and more important because of the increasing demand for low power applications. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

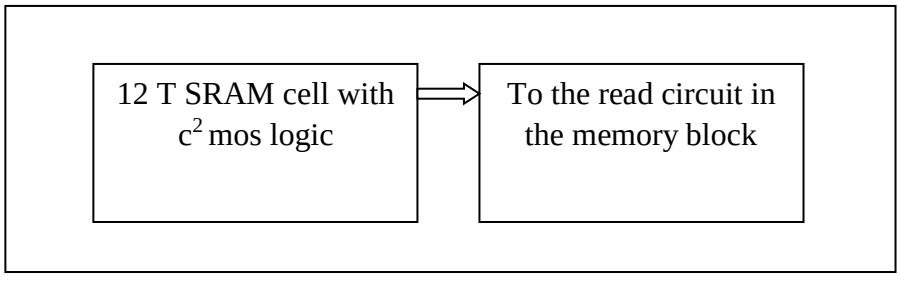

Figure 4.3 10T SRAM cell with c^2mos logic

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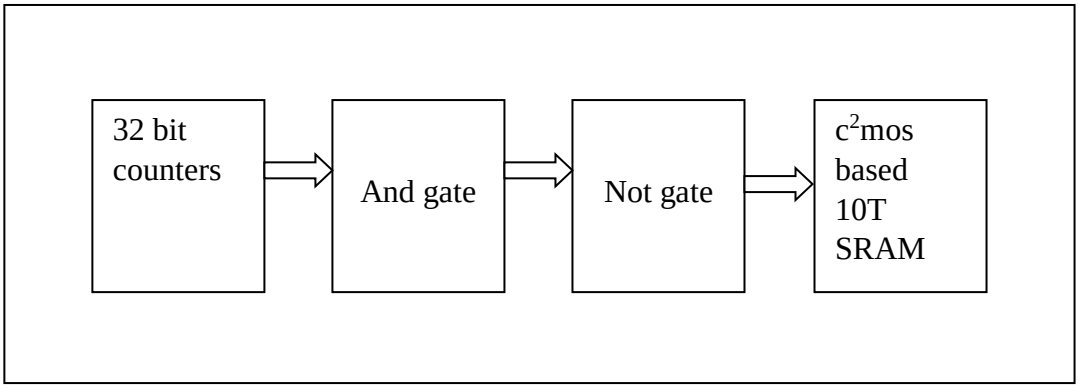

Figure 4.4 Modified read circuit in the memory block

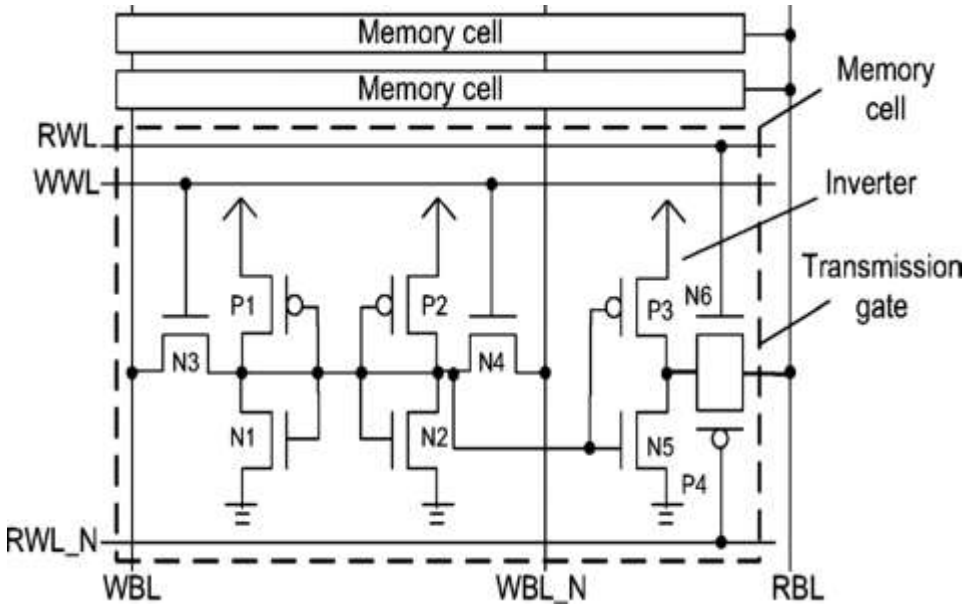

Figure 5.3 10T SRAM cell

The memory block consists of read circuit. The read circuit consists of memory cells. The memory cell used is 10T SRAM cell. The designed 10T SRAM cell is used in the read circuit of the memory block. The 10T SRAM cell consists of conventional 6t sram cell. An inverter and transmission gate is for read operation. N3 and N4 Transistors are called access transistors. These access transistors are connected to WWL. Depending on the WWL value and WBL values read and write operation will be performed. By enabling write enable (w_en) and read enable write and read operation will be performed. Low power, high speed 10T SRAMs are used in the memory cell of the fpga that supports fast read operation and large bit-width.10T SRAM cell includes a conventional 6T SRAM cell, a readout inverter and a transmission gate for the read port. Write operation can be accomplished as in a conventional 6T SRAM. For read operation, since the readout inverter is able to fully charge/discharge the read bit line, the precharge scheme is not required. Therefore, the voltage on the bit line does not switch until the readout datum is changed.

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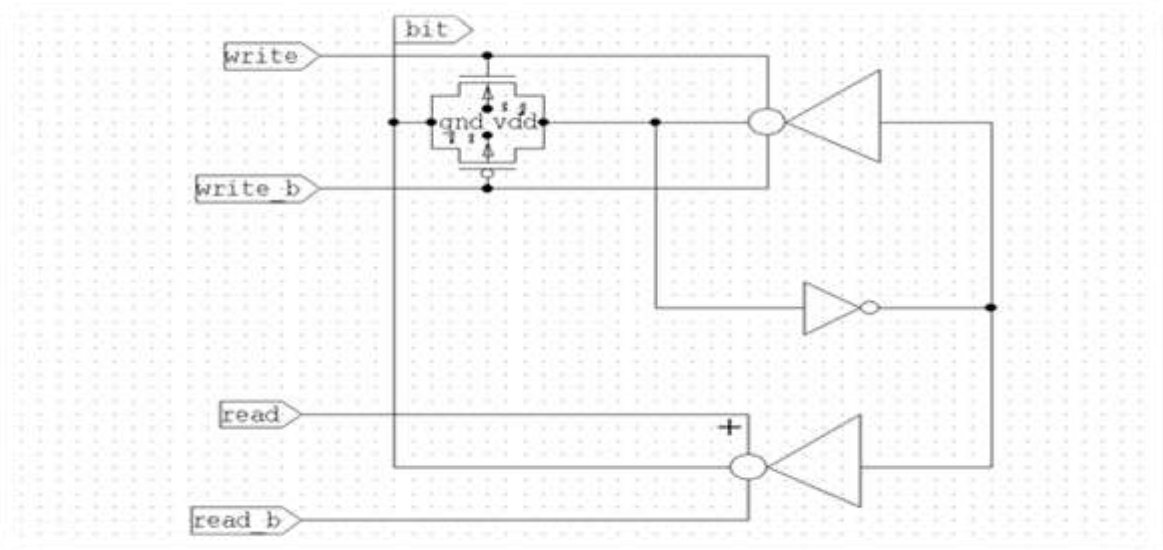

Figure 6.2 10T SRAM cell

In the proposed system the read circuit of the memory block is implemented using 10T SRAM cell. The 10T SRAM cell is shown in the fig 6.2.The 10T SRAM memory cell is designed using c^2mos logic. The c^2mos logic Circuit is shown in the fig 6.3.

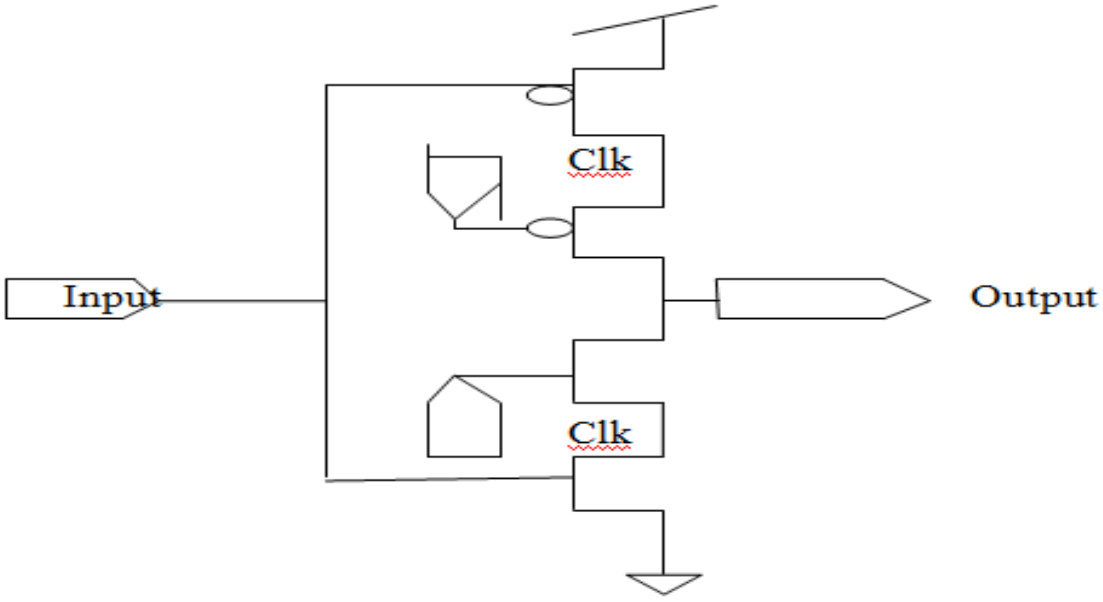

Figure 6.3 c^2mos logic circuit

The c^2mos logic involves clocking circuit. The output value depends on both the input value and the clock pulse. The advantage of 10T cell over 10T cell is, in the 10T cell the switching activities is reduced and delay is reduced. The 10T SRAM cell includes two c^2mos logic circuit, transmission gate and cmos inverter. The transmission gate is used to give some delay when the inputs arrive at the same time. The inverter is for changing of the bits.

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READ CIRCUIT IN THE MEMORY BLOCK

The modified read circuit is shown in figure 6.5. The proposed read circuit of the memory block is implemented using counters. The existing system consists of 32 bit shift registers. The proposed system consists of D flipflop to work it as counters..

Result and discussion

- Memory Cell
- Read Circuit in Memory block
- FPGA block.

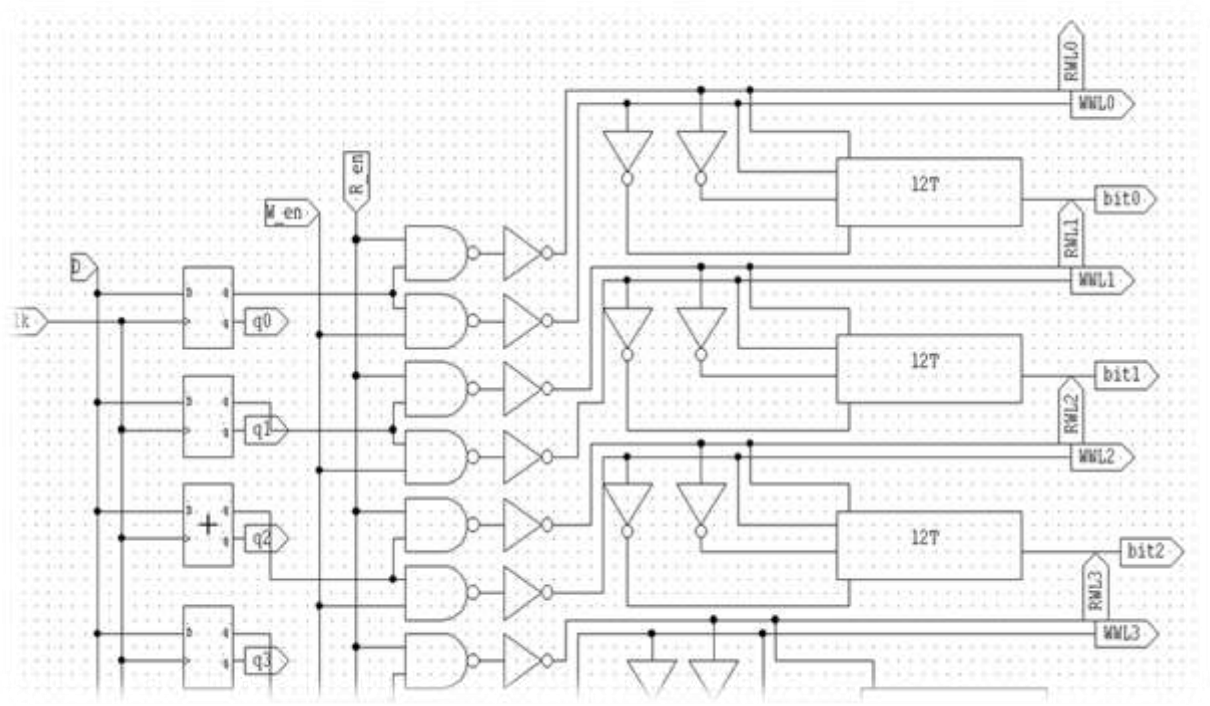

Figure 6.5 Modified read circuit of memory block

8.1 MEMORY CELL

The existing system memory cell and the proposed cell power results are compared[1]. Depending on WWL, WBL value write and read operation will be performed in the 10T SRAM cell.

8.2 READ CIRCUIT IN THE MEMORY BLOCK

The designed 10T SRAM cell is placed in the read circuit of the memory block. The waveform shows the output obtained during read and write operation. The read circuit of existing system makes use of shift registers. The read circuit of proposed system makes use of counter[5]

8.3 FPGA BLOCK

The existing sytem stimulated FPGA block power results is shown in figure8.5. The proposed system stimulated FPGA block is shown in figure 8.6. The FPGA block includes

- Memory cell which will be present in the read circuit memory block
- Switch block which includes switch matrix
- Logic block
- Logic block consists of logic elements

All the blocks are designed which forms the stimulated FPGA block results.

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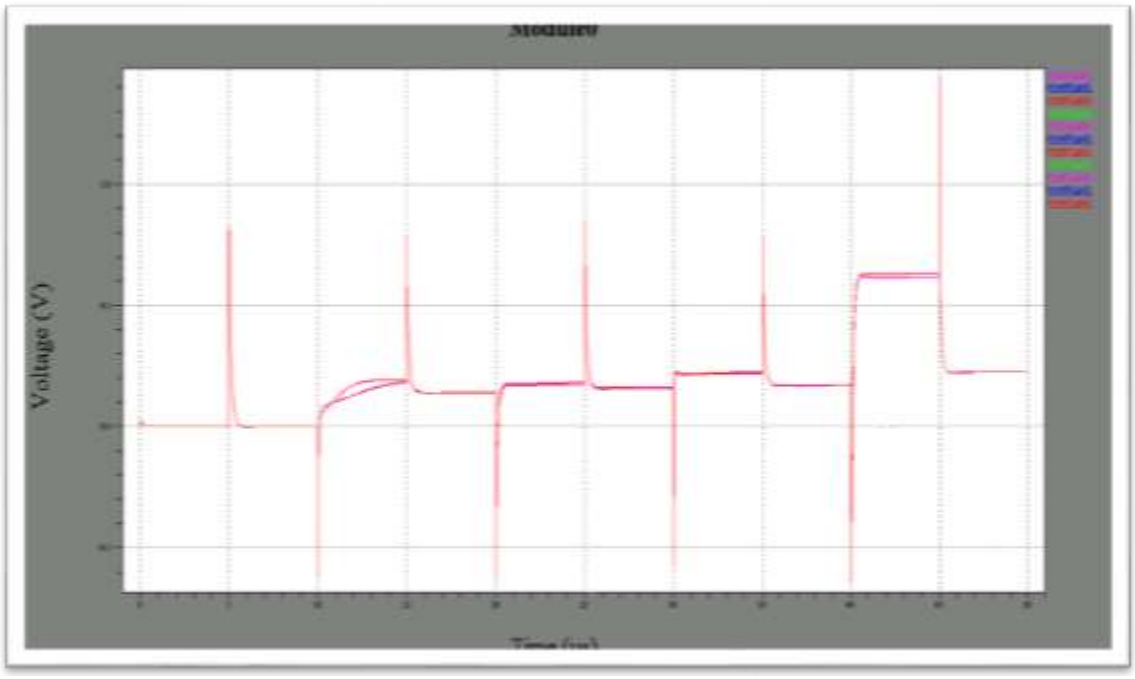

Figure 8.5 Power results of FPGA block based on 10T SRAM cell

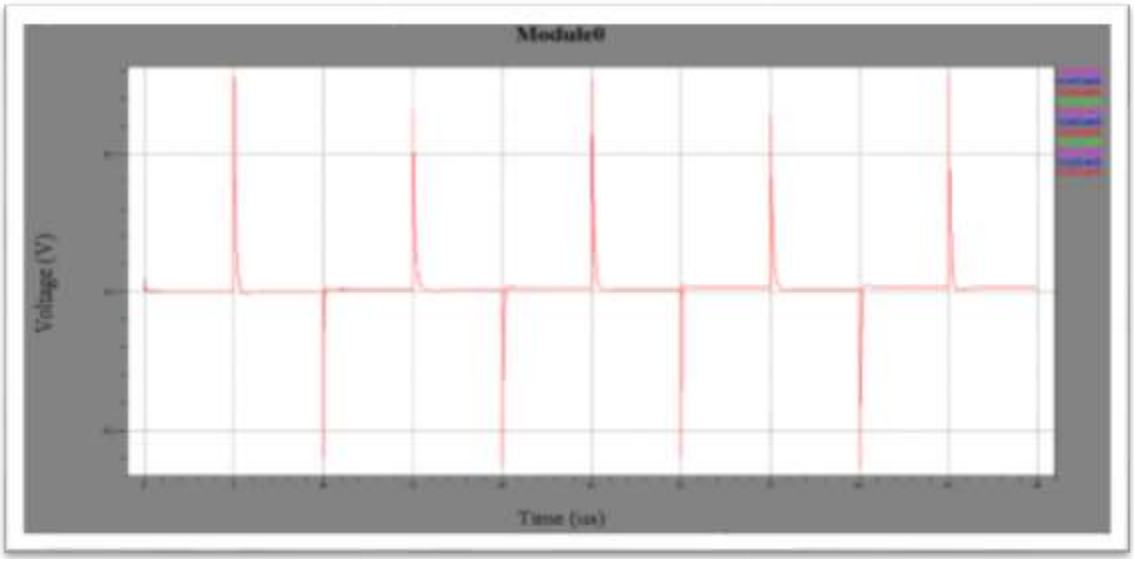

Figure 8.6 Power results of Modified FPGA block based on 10T SRAM cell

8.4 COMPARISON TABLE FOR EXISTING AND PROPOSED SYSTEM

Table 8.1 comparison table for existing and proposed system

Parameter Exists	10T SRAM cell	12T SRAM cell	Read circuit of the memory block	Modified read circuit of the memory block	FPGA block	Modified FPGA block

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Average power(watts)	3.423	0.532	15.96	8.83	0.503	0.409
Power delay product(watts per sec)	$2.35*10^{-3}$	$3.84*10^{-7}$	$1.98*10^{-3}$	$8.11*10^{-5}$	$1.17*10^{-3}$	$2.34*10^{-4}$
Energy delay product(joules per sec)	$5.52*10^{-6}$	$1.47*10^{-13}$	$3.940*10^{-6}$	$6.577*10^{-9}$	$2.89*10^{-6}$	$5.47*10^{-8}$

CONCLUSION

Low power design is the major concern in the electronics industry. The circuit designed should have low power consumption. Since memories contribute to the major portion of the power dissipation, work is made to reduce power consumed in the memory of the FPGA. The proposed system makes use of 10T SRAM memory cell which is designed using c^2mos logic. The use of 10T SRAM cell is to reduce switching activities and delay .The designed 10T SRAM cell is used in the read circuit of the memory block. The 10T SRAM cell used reduces the average power consumed by 2.89 percent. The proposed read circuit is implemented using counters to access the bits faster. Logic block is implemented. Average power, product delay product, energy delay product of the designed blocks is calculated. The existing system and proposed system results are tabulated and compared.

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