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HIGH SPEED SYSTEM USING VEDIC MATHEMATICS - A SURVEY

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ABSTRACT

In the world of technology knowingly or unknowingly we use Vedic Sutra.
Likewise, many Vedic sutras are used in multiplier unit of computer. It will give faster results, which is very much required in various applications like cryptographic algorithms, image processing applications. Traditional methods used for multiplication, division require more time as compared to Vedic methods. UrdhvaTiryagbhyam, Nikhilam sutra are used for multiplication purpose. It require less time, power and give results faster.

INTRODUCTION

Multipliers are key components of many high performance systems such as FIR filters, Microprocessors, Digital Signal Processors, etc. A system's performance is generally determined by the performance of the multiplier, because the multiplier is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue [18].
Vedic Mathematics is one of the most ancient methodologies used by the Aryans in order to perform mathematical calculations [11]. This consists of algorithms that can easily solve large arithmetic operations to simple mind calculations. Vedic mathematics approach is totally different and considered very close to the way a human mind works. The efforts put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to introduce
Vedic Mathematics to the commoners as well as stream line Vedic Algorithms into 16 categories [12] or Sutras needs to be acknowledged and appreciated. The Urdhva Tiryakbhayam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved.

With the advancement in the VLSI technology, there is an ever increasing quench for portable and embedded Digital Signal Processing (DSP) systems. DSP is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Traditional method used for arithmetic operation take longer time for processing. It includes different methods like booth, array method, carry save, Wallace tree etc. Also these methods are not very efficient in speed, power and area. Vedic Methods (sutra) require lesser step to solve arithmetic operation.
Reversible logic [13] is one of the most vital issue at present time and it has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. It is not possible to realize quantum computing without implementation of reversible logic. This paper provides reviewed of various papers that used Vedic Mathematical sutra for designing multipliers.

VEDIC SUTRAS

The India has a great history regarding ancient books like RAMAYAN, GEETA, VEDA'S and lots of more. One of them is Veda, there are many parts of Veda and one is related to mathematics which will we called as Vedic

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Mathematics. The word ―Vedic‖ is derived from the word ―Veda‖ which means that it contains all the knowledge of that field or we can say that it is a store-house of all the knowledge. Vedic Mathematics is mainly based on 16 Sutras which covers various branches of mathematics like Arithmetic, Algebra, Geometry, etc. [11], [15]. In the period of 1884-1960 the Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja comprises all the Vedas together and gave its mathematical explanation while discussing it for various applications. After extensive research in Atharva Veda Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae). All these sutras are in Sanskrit and it is very difficult to translate, after all these are constructed by Swamiji himself. Because of Swamijis hard work for us Vedic Mathematics is not only mathematical wonder but also it is logical. Vedic mathematics has phenomenal characteristics, because of its easiness and applicable to all types Vedic maths has already crossed the boundaries of India and it is a very interesting topic of research in abroad. Especially, the methods of basic arithmetic are extremely simple and powerful because of these easiness it is use full in every filed [16], [17]. The following are the 16 main sutras or formulae of Vedic math and their meaning in English *(Anurupye) Shunyamanyat* – If one is in ratio, the other is zero.

1. *Chalana-Kalanabyham* – Differences and Similarities.
2. *Ekadhikina Purvena* – By one more than the previous one.
3. *Ekanyunena Purvena* – By one less than the previous one.
4. *Gunakasamuchyah* – The factors of the sum is equal to the sum of the factors.
5. *Gunitasamuchyah* – The product of the sum is equal to the sum of the product.
6. *Nikhilam Navatashcaramam Dashatah* – All from 9 and the last from 10.
7. *Paraavartya Yojayet* – Transpose and adjust.
8. *Puranapuranabyham* – By the completion or noncompletion.
9. *Sankalana-vyavakalanabhyam* – By addition and by subtraction.
10. *Shesanyankena Charamena* – The remainders by the last digit.
11. *Shunyam Saamyasamuccaye* – When the sum is the same that sum is zero.
12. *Sopaantyadvayamantyam* – The ultimate and twice the penultimate.
13. *Urdhva-tiryakbyham* – Vertically and crosswise.
14. *Vyashtisamanstih* – Part and Whole.
15. *Yaavadunam* – Whatever the extent of its deficiency.
16. *(Anurupye) Shunyamanyat* – If one is in ratio, the other is zero.

RELATED WORK

Honey Durga Tiwari et al. for low power and high speed architecture designed a multiplier and square architecture .They used Vedic sutra like Urdhva Tiryakbyham and Nikhilam sutra can be efficiently used for two large multiplication by reducing it to two small number multiplication. The proposed method was more efficient in terms of time delay and speed as compared to methods like Booth and Array multipliers. [1]

M.Ramalatha et al. proposed a design for high speed energy efficient ALU. Vedic mathematic technique were implemented for this purpose. The designed high speed multiplier support co-processer which reduces load of processor. They used Urdhav Tiryakbyham sutra and showed that Urdhav Tiryakbyham sutra reduces the number of unwanted multiplier and produces intermediate result parallely. [2]

Devika Jain et al. proposed a low power design for multiplier accumulator unit (MAC). Their approach is more suitable for DSP as it require low power. MAC multiplier is based on Vedic sutra Urdhav Tiryakbyham. For coding VHDL was used. Comparison was made between proposed high speed vedic multiplier and modified Booth Wallace multiplier. It was found that Vedic multiplier is more efficient than with modified Booth Wallace multiplier compared ones. [3]

Akhalesh K Itawadiya et al. realise the importance of multiplication in DSP operation eg correlation. They gave very easy and simple method for DSP operation for small length of sequence. A sutra from ancient Vedic mathematics called Urdhav Tiryakbyham was used for doing this multiplication. These operation were implemented in MATLAB and proved that this method require less processing time as compared to inbuilt function of MATLAB. [4]

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Sushma R. Huddar et al. design and developed an efficient architecture for performing mix columns and inverse mix columns operation which is important in Advanced Encryption Std (AES) method of cryptography. They identified need of high speed cryptographic algorithm used in secure transaction. They used Urdhav Tiryakbyham sutra from ancient Vedic mathematic for this purpose. Their method doubles the time speed as compared to traditional method used for this purpose. This method was developed using Xilinx software.

[5] R. Thamil Chelvan et al. design and implemented fixed and floating point division using dhvajanka sutra from Vedic mathematic. Designed technique is used in RSA cryptographic algorithm. Basically RSA deals with division operation and their method using Vedic sutra as compared with conventional division algorithm showed greater efficiency. For coding purpose VHDL was used.

[6] Diganta Sengupta et al. proposed an algorithm for fast BCD division based on ancient Vedic mathematics. Nikhilam and Parvartya sutra were used for these purpose. Thus proved that execution time does not depend upon size of dividend or divisor but no. of remainders normalization required. Traditional method uses successive subtraction method which are time consuming. Proposed method is much faster as it involves addition and negative operation. [7]

Pavan Kumar et al. designed 8-bit Vedic multiplier using barrel shifter which require only one clock cycle for 'n' no. of shifts. It was develop using Nikhilam sutra. They used barrel shifter at different level of which drastically reduced the delay when compared with conventional multiplier. Also there was improvement in speed which is suitable in image processing, Arithmetic logic unit, VLSI signal processing. The design was verified and implemented using FPGA and ISE simulator. [8]

Rakshith saligram et al. aim to enhance the performance of previous reversible logic design. They used Total Reversible Logic Implementation Cost (TRLIC) to aid their proposed designed. They proved that proposed designed can be efficiently used in designing FFT's Filters and application likes wireless communication, image processing and software defined radios. They used UT sutra from ancient Vedic mathematics for this purpose. They proved that lower TRLIC, lower is quantum cost hence lower is the delay and hence vice versa. The designed was tested using Xilinx software. [9]

Surabhi Jain et al. had deep study of Vedic mathematics. Designed binary division algorithm as well as high speed deconvolution algorithm using Vedic sutra which is suitable for image processing application. Traditional division is length, bulky and difficult arithmetic operation. It require large space area and time complexity. For binary division they used Nikhilam sutra and Parvarty sutra from Vedic mathematics. Time delay and complexity both were improved using both sutra. Algorithm were tested using VHDL and Xilinx ISE. [10]

URDHVA TIRYAKBHAYAM

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed. The digital logic implementation of the 2X2 Urdhva Tiryakbhayam multiplier (Cross Multiplication) is as shown in Figure.3a.

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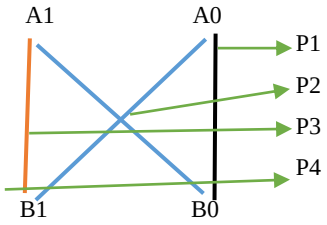

*Figure 3a. Cross Multiplication of 2*2 Multiplier*

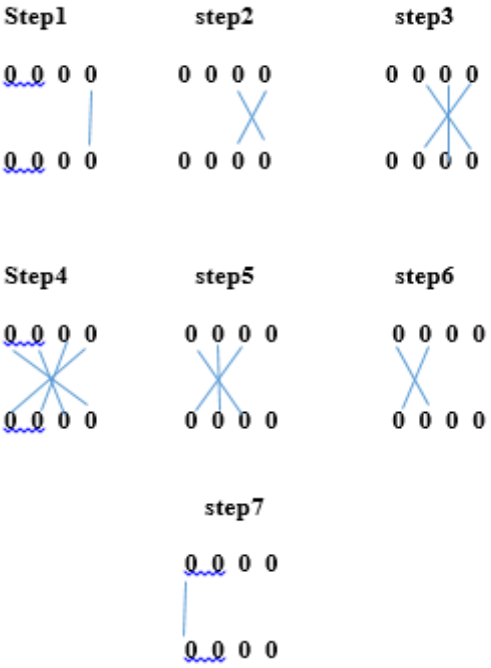

Figure 3b Line Diagram for Multiplication of two 4-bit number

NIKHILAM SUTRA

Nikhilam Sutra means "all from 9 and last from 10" Nikhilam sutra is applicable for all types of multiplication but it is more efficient when number involved large numbers. In this method it finds out the compliment of the large number from its nearest bases of 10, 100, 1000 to perform multiplication operation on it. The multiplication procedure using Nikhilam involves minimum mental manual calculation, which in turn will lead to reduce number of step in computation, reducing the space area, saving more time for computation. The number taken can be either less or more than the base considered. Let us illustrate this sutra by considering the multiplication of two decimal numbers (96 * 94) where the chosen base is 100 which is nearest to and greater than both these two numbers.

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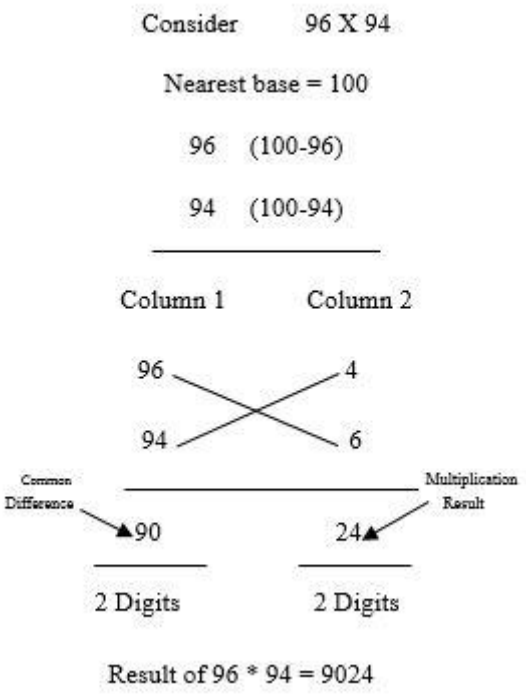

Multiplication using Nikhilam Sutra

RHS product can be obtain by simply multiplying the number of column 2 (4*6=24). The LHS product can be obtain by cross subtracting the second number of column 2 from the first number of column 1 and vice versa i.e (96-6=90) and (94-4=90). The final result obtained by concatenating RHS and LHS (Answer=9024). [12]

Sr. No.	Title of Paper	Method/ Sutra from Veda	Features
1	Multiplier Design Based on ancient Indian Vedic Mathematics	Urdhva Tiryakbhayam and Nikhilam sutra	Less design and delay area, Faster Multiplier and square architecture
2	High Speed Energy Efficient ALU Design using Vedic Multiplication techniques	Urdhva Tiryakbhayam	Parallel generation of intermediate product.
3	Vedic Mathematics Based Multiply Accumulate Unit	Urdhva Tiryakbhayam	Binary number multiplication, Realized easily on silicon due to regular and parallel structure.
4	Design a DSP Operation using Vedic Mathematics	Urdhva Tiryakbhayam	Vedic mathematics based DSP requires less processing time than inbuilt MATLAB function, Gives better result.

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5	Novel Architecture for Inverse Mix Column for AES using Vedic Multiplication on FPGA	Advance Encryption Standard (AES) Urdhva Tiryakbhayam	High Speed and Low on chip area
6	Implementation of fixed and floating point division using Dhvajanaka sutra	Dhvanjanaka Sutra	Used in division of RSA encryption/decryption, efficient in terms of area and speed.
7	A New Paradigm In Fast BCD Division Using Ancient Indian Vedic Mathematics Sutras	Nikhilam and Parvartya sutra	The computation time required by the Vedic Division Algorithm is approximately constant irrespective of size of the dividend.
8	FPGA Implementation of High Speed Vedic multiplier using barrel shifter	Nikhilam Sutra	Barrel shifter were used to reduce the delay , improvement in speed
9	Optimized Reversible Vedic Multiplier for High Speed Low Power Operations	Urdhav tiryakbhayam	Decreasing TRLIC, delay was reduced, Useful in applications likes wireless communication, image processing and software defined radios.
10	Binary Division Algorithm and High Speed Deconvolution Algorithm (Based on Ancient Indian Vedic Mathematics)	Nikhilam, Parvarty Sutra	Used for calculating deconvolution, reduced time delay and complexity

CONCLUSION

In this paper, we have focus on different Vedic sutra used for designing various multipliers. Vedic mathematics sutra are used in different place of different arithmetic operation like division, multiplication, square and cube etc. Used in applications like digital signal processing, image processing, cryptography and computation of heavy calculation. More research and study in the field of Vedic mathematic and their sutras used in multiplier will give better result and have a lot of scope in different field.

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