ISSN 2349-6193
Impact Factor: 2.805

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DIFFERENT SUBSTRATE LEVEL NOISE IN MIXED SIGNAL INTEGRATED CIRCUITS

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Keywords: Microfiber, fabric structure, comfort properties, air permeability, water vapour permeability, thermal resistance.

ABSTRACT
In mixed-signal integrated circuits analog and digital circuits share the same silicon substrate material. When a digital circuit Is switching, the voltages in the circuit nodes change rapidly and switching noise is generated

INTRODUCTION

1.1 Substrate Noise

In mixed-signal integrated circuits analog and digital circuits share the same silicon substrate material.When a digital circuit Is switching, the voltages in the circuit nodes change rapidly and switching noise is generated. The noise is spread through the substrateandis received by other circuits, which is demonstrated in Fig. 1.1. The noise in the substrate is referred to as substrate noise. Due to the substrate noise the performance of sensitive analogcircuits is seriously degraded when analog and digital circuits are integrated.Substrate noise that originates from digital circuits is generally orders of magnitude larger than device noise(i.e.,thermal,flicker and shot noise)in high-speed mixed-signal circuits . Hence, the device noise is generally a minor problem compared to substrate noise in the design of an analog circuitfor a mixed-signal IC.

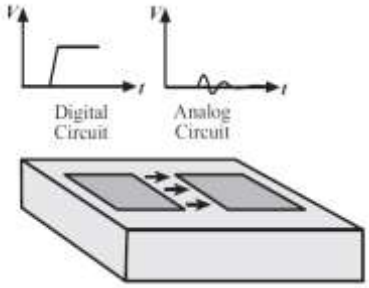

Figure 1.1: substrate noise in a mixed-signal circuit

1.2 Substrate Types in CMOS Technologies

In normal CMOS technologies, there are mainly two types of substrate that are used. The first substrate type consists of a thick layer of heavily positively doped silicon (*p*+) with thin lightly positively doped silicon (*p*-) on top as illustrated in Fig. 1.2(a). This kind of technology is referred to as epitaxial substrate or heavily doped substrate. The thickness of the epitaxial layer is typically about 10 mm. The thickness of a chip is commonly from 300 mm to 600 mm. In modeling, the layer of the heavily doped silicon may be approximated to a single node due to its high conductance. As a consequence, the substrate noise in heavily doped substrates tends to be uniform over the chip area. Historically, heavily doped substrates have been widely used due to the low risk of latch-up. The second substrate type is the uniform lightly doped substrate, which is illustrated in Fig. 1.2(b). In this substrate the resistivity is higher than in the heavily doped substrate, due to that the doping level is lower. Therefore, the substrate coupling is smaller in the lightly doped substrate. For this reason the lightly doped substrate is considered to be a better choice for mixed-signal ICs than the heavily doped substrate. Silicon on insulator (SOI) is a technology where a thin-film of silicon is placed on a buried insulating layer (e.g. silicon oxide). Under the insulating layer a thick layer of lightly doped silicon is commonly used. The profile of an SOI substrate is illustrated in Fig. 1.3. The SOI technology results in smaller parasitic than a conventional CMOS technology, since the PN junctions are shallower in SOI showing to the thin-film. Hence, the circuits implemented in the SOI technology is in general somewhat faster and less power consuming than in conventional bulk technologies. The insulator layer also reduces the coupling between circuits, which is beneficial in mixed signal applications. For these reasons SOI is believed to be widely used in the future.

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1.3 Substrate Modeling

To predict the coupling between circuits that are placed on the same chip, a proper substrate model is required. Typically the height of a chip is about 300 to 600 mm, which is significant with respect to the horizontal dimensions of a chip. Consequently, in modeling of the electrical properties of a lightly doped substrate the model must be based on the three dimensions in space.

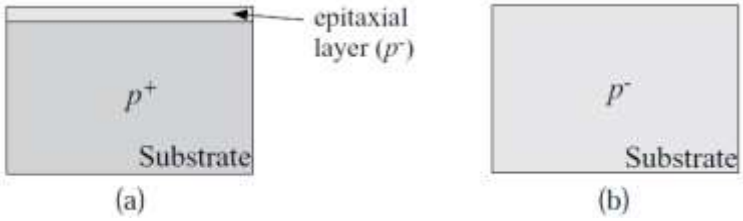

Figure 1.2: (a) Heavily doped substrate, and (b) lightly doped substrate.

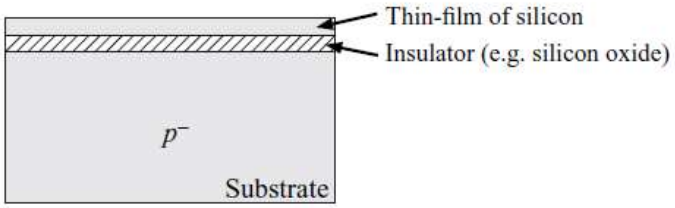

Figure 1.3: Silicon-on-isulator (SOI) substrate

For low frequencies (below a few GHz) the substrate is mainly resistive. For high frequencies (typically above a few GHz) the dielectric behavior of the substrate comes into play. Hence, for these frequencies the capacitive coupling in the substrate must be added to the substrate model. The coupling through a substrate is both resistive and capacitive. However, for low frequencies the substrate can be approximated as purely resistive. The substrate is mainly resistive for frequencies up to

$$f\mathrm{c} = \frac{1}{2\pi\rho_{sub}\varepsilon_{si}} \qquad 1.1$$

Where ρ_{sub} and ε_{si} are the resistivity and the permittivity of the substrate, respectively . For example, assuming a lightly doped substrate with a resistivity of0.10 M Ω yields according to (1.1) that the substrate is mainlyresistive for frequencies up to 15 GHz. Neglecting the capacitive coupling, the model is reduced from an RC net to a resistor net. Consequently, the complexity of the net is reduced, which saves time in simulations. A resistive model of the substrate consisting of *N* ports (i.e., substrate areas) and a number of intermediate nodes can be reduced without lack of accuracy. For instance, a reduced but still full model contains only the *N* ports and *M*-resistors that all are connected so that each port is connected with all the other ports. Hence, in a full model with *N* ports the required number of resistors is

$$M = \sum_{j=1}^{N-1} j = 1 + 2 + 3 + \cdots + (N-1) = \frac{N}{2}(N-1). \quad 1.2$$

For a substrate with an uniform doping level, it is straightforward to extend a resistive model to include the capacitive coupling. The coupling through the substrate can be modeled with elements consisting of a resistor in parallel with a capacitor. The ratio between the impedance from the resistive part R and the capacitive part $\frac{1}{\omega c}$are

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always equal for a given frequency. Hence, for a determined resistive coupling the capacitive coupling can easily be calculated by using

$$C = \frac{\rho \rho_{sub} \varepsilon_{si}}{R} 1.3$$

This means that a modeling technique of a uniformly doped substrate that can accurately determine the resistive coupling also can accurately determine the capacitive coupling. In the research area of substrate modeling there are some different objectives. Some modeling techniques are focusing on achieving high accuracy while others are focusing on fast estimation with some relaxation in accuracy. For instance, the substrate models based on the finite element method (FEM) and finite difference method (FDM) can be very accurate but slow in computation, while the boundary element method (BEM) generally is faster. Using FEM, a discretization of the substrate is made by a mesh of elements. The partial differential equations are then solved for each element. Using FDM, the substrate is divided into a number of nodes and the electric field vector between adjacent nodes is approximated using a finite difference operator. In BEM each port (i.e., surface area) are divided into a number of smaller areas. Laplace's equations are then solved with the boundary conditions using Green's function. The boundary element method (BEM) is generally faster than FEM and FDM, but it has some limitations in accuracy as soon as regions with different doping (e.g., n-wells) are included. In FEM and BEM are combined to obtain a fast and still accurate model.

1.3.1 A Substrate Model Derived from Maxwell's Equations

The basic Maxwell's equations can be used to describe the substrate. However, a closed form solution to these equations does not exist as soon as geometries of different doping levels (e.g., n-wells) are included in the substrate or different layers of the substrate have different doping levels (i.e., on-uniform substrate doping).To overcome this problem the substrate may be divided into a number of smaller elements where each element is assumed to have a constant doping level. Hence, the resistivity and the permittivity are assumed to be constant within each element. The equations can then be solved for the element so that a model of each element is obtained. Ignoring the magnetic field, a simplified form of Maxwell's equations can be written as.

$$\varepsilon \frac{\partial}{\partial x}(\nabla E) + \frac{1}{\rho} \nabla E = 0 \qquad 1.4$$

Here, is the electrical field, the resistivity, and is the permittivity of the silicon within the element. A cube shaped element with the volume *V* and the side 2*d* is shown in Fig1.4. The closed surface of the cube is denoted *S*. Gauss' law gives that the divergence of the electrical
field in a point equals a constant .Hence ,the divergence in mode I in the cube is .

$$\nabla . E = k. \quad 1.5$$

We integrate $\nabla . E$over the volume v formed by the cube fig 1.4 and then rewrite (1.5)as

$$\int_V \nabla . E dV = \int_V K dV = 8\mathrm{d}^3 k \qquad 1.6$$

The divergence theorem gives

$$\int_V \nabla . E dV = \int_s E ds \qquad 1.7$$

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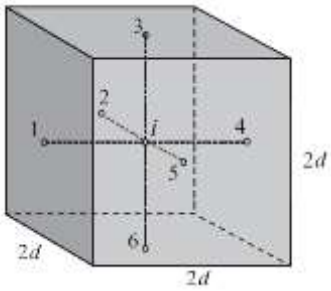

Figure 1.4 :A cube shaped substrate element

Therefore,

$\nabla . E = 1/8\mathrm{d}^3 \int_s Eds$ 1.8

The integral in(1.8) can be approximated as

$\int_s Eds = \sum_{j=1}^{6} E$ ij $4\mathrm{d}^2$1.9

and electrical field from node j to i can be subsitute

Hence

$\nabla . E = 1/8\mathrm{d}^3 \sum_{j=1}^{6} \frac{Vi-Vj}{\frac{d}{2}} 4\mathrm{d}^2 = \sum_{j=1}^{6} \frac{Vi-Vj}{\mathrm{d}^2}$ 1.10

Using(1.10) in (1.4) gives

$$\frac{1}{\rho}\sum_{j=1}^{6} \frac{Vi-Vj}{\mathrm{d}^2} + \varepsilon \frac{\partial}{\partial t}\left[\sum_{j=1}^{6} \frac{Vi-Vj}{\mathrm{d}^2}\right] = 0 \quad 1.11$$

We rewrite (1.11) gives.

$$\sum_{j=1}^{6}\left[\frac{(Vi-Vj)}{R} + C\left(\frac{\partial Vt}{\partial t} - \frac{\partial Vt}{\partial t}\right)\right] = 01.12$$

Where and. Equation (1.1) corresponds to that the sum of the currents flowing into node *i* is zero. The resulting model is shown in Fig.1.5, where each impedance from a surface to the middle node *I*is modeled as a resistor in parallel with a capacitor with the values *R* and *C*, respectively. For high frequencies (above ten GHz) this model can be expanded to include loss in the dielectric behavior of the substrate to increase the accuracy. In a resistor is added in series with the parallel coupled capacitance and resistance to make the model valid for frequencies up to 40GHz.

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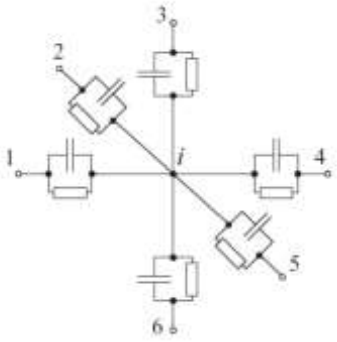

Figure 1.5: A model of the cube shaped substrate element.

To obtain reliable results from a model, the mesh should be fine (i.e., small elements) in regions where the gradient of the doping level is large and also where the gradient of the electrical field is large. Due to the large number of nodes required in the mesh, it is not suited for hand calculations and therefore a simulator is required. By using a circuit simulator (e.g., SPICE) the coupling between different areas of the substrate can be analyzed.

1.4 Simultaneous Switching Noise

1.4.1 Cause of Simultaneous Switching Noise

The parasitic impedance in the power supply interconnects between on-chip and off-chip plays a big role in ICs. The parasitics are inductance and resistance coming from traces (e.g., lead frame) and bonding wires (or solder balls) within the package. Normally, the critical parasitic of IC packages is the inductance in the current paths. Parasitic capacitances and typically decoupling capacitors are present between the on-chip positive power supply and the ground line. The sum of these capacitances can be modeled as a lumped capacitor C_{eff}. When digital circuits are switching, large current peaks are generated. The current peaks together with the parasitic inductance and the resistance generate voltage drops on the on-chip power supply voltage. The drop on the on-chip power supply voltage is

$$V\ supply = L\text{eff}\ \frac{dI}{dt} + Reff\ \text{I} \qquad 1.13$$

where*Leff*and *Reff*are the parasitic inductance and resistance of the power supply current path. The dominant part of the impedance is in general the inductance due to the large values ofdI/dt. When a current peak occurs in the power supply, a damped voltage oscillation is initiated . For simplicity, let L_1=L/2,R_1=R/2 and C_{eff}=C, giving L_{eff} = LandR$_{eff}$=R .The damped oscillation, after the appearance of the current spike,can be described by

$$V\ supply = e^{-\vartheta\omega 0t}\ \text{k}\sin(\omega\text{t} + \theta) \qquad 1.14$$

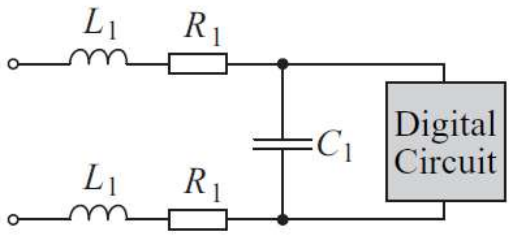

Figure 1.06: A simple model of the impedance in the power supply lines of a digital circuit.

Where

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$$\vartheta = \frac{R}{2}\sqrt{\frac{C}{L}} \qquad 1.15$$

$$\omega o = \frac{1}{\sqrt{LC}} \qquad 1.16$$

And

$$\omega = \omega o\sqrt{1-\vartheta} \qquad 1.17$$

$\vartheta$is known as the damping factor which in general is less than unity Ø and k depend on the values of *R*, *L*, and *C* and the waveform of the current spike. In a digital circuit, the number of generated current peaks and their distribution in time depend on which nodes that are switching within the circuit. Therefore, the waveform and the frequency content of the power supply voltage are data dependent. The damping of the sinusoidal is

$$\vartheta\omega o = \frac{R}{2L} \qquad 1.18$$

Hence, the smaller *L* and the larger *R* the faster is the attenuation of the voltage fluctuation. A smaller *L* also results in a smaller initial voltage drop according to (1.13). On the other hand a larger *R* results in an increased initial voltage drop. The frequency of the damped oscillation is, according to (1.14) and (1.17),

$$f\ osc = \frac{\sqrt{1-\vartheta^2}}{2\pi\sqrt{LC}} \qquad 1.19$$

However, the oscillation frequency is often approximated with

$$f\ osc \cong \frac{1}{2\pi\sqrt{LC}} \qquad 1.20$$

The described voltage fluctuation on the power supply is known as simultaneous switching noise (SSN) or dI/dt - noise. In digital designs, SSN can result in malfunction or degraded performance. In mixed-signal ICs the performance of analog circuits is seriously degraded by the SSN that is spread through the substrate.

1.4.2 Switching of an On-Chip Load

In Fig. 1.07, charging of an internal node within a digital circuit is for simplicity illustrated by an inverter. The parasitic capacitances in the node are modeled by C_1 and C_2. While C_1 is charged, C_2 is discharged. The current discharging C_2 is only within the loop $I_{internal}$, as illustrated in Fig. 1.07. Therefore, $I_{internal}$does not contribute to the total SSN. The charge required from the power supply due to the charging of C_1 is $C_1 V_{DD}$. This charge is taken from the power supply whose current is denoted I_{power}. As seen in Fig. 1.07, the currents through the positive power supply and the ground linear equal. Hence, the voltage transients on the power supply lines are antisymmetrical if $Z_1 = Z_2$. The discharging of the internal node is illustrated in Fig. 1.08. During the discharging a similar behavior can be seen

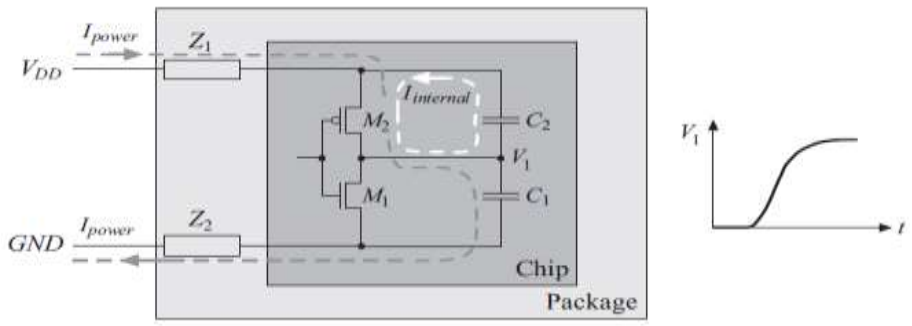

Figure 1.07: Charging of an on-chip node in a digital circuit

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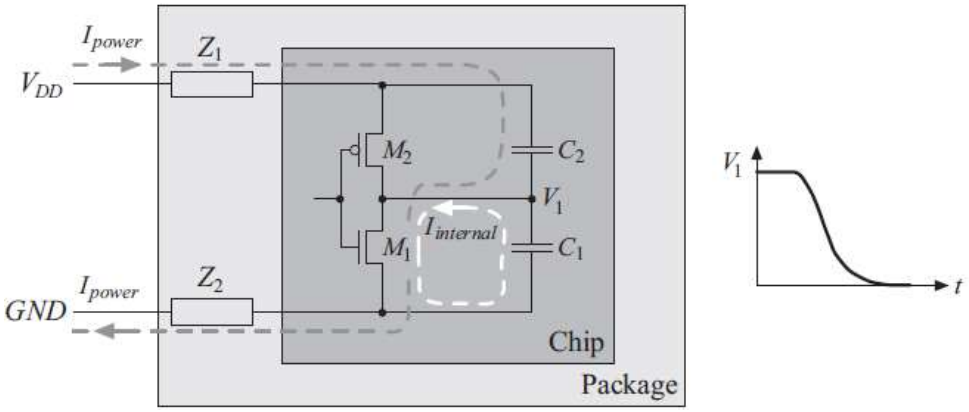

Figure 1.08: Discharging of an on-chip node in a digital circuit.

as during the charging. The charge taken from the power supply is C_2VDD . The discharging current of C_1 is local on chip and is denoted $I_{internal}$in Fig. 1.08, while the charging current of C_2 goes through the power supply lines. Hence, voltage transients are seen on the power supply lines both while charging and discharging of an internal node.

1.4.3 Switching of an Off-Chip Load

To drive a digital output of an IC, cascaded inverters are commonly used as a driver. The output load consists of the parasitic capacitance of the bonding pad, the inductance and capacitance of the interconnect from on-chip to offchip, and the load on the printed circuit board (PCB), e.g., wire trace plus the input of another IC. The current required to charge or discharge an off-chip load can be large, especially in the case of a high-speed communication. As a consequence, the output drivers of a digital circuit generally generate a considerable amount of the total SSN. The power supply lines for the output buffers are normally separated from the power supply lines for the chip core. Hence, the current paths of the output drivers differ from the paths of the power supply to the chip core. For instance, the current path of a single ended output inverter is data dependent. While charging, the current path is through the positive on-chip power supply line and through the output load, which is illustrated in Fig. 1.09. In this case, the current through the on-chipground line is approximately zero. While discharging, the current path goes through the ground supply line and through the output load. Therefore, the assignment of pins for power supply of single ended output buffers is more complicated

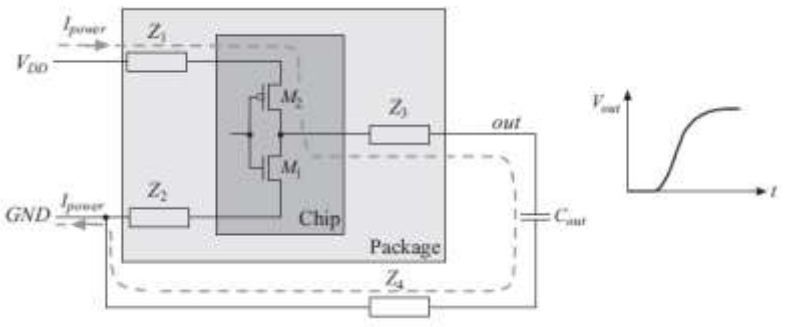

Figure 1.09: Charging of an off-chip load.

than for the chip core. However, if a differential signaling is used for an output, the current path is always through the differential pair of interconnects as in low voltage differential signaling (LVDS), Inexperiments were made where the number of simultaneous switching output drivers was varied. The conclusion was that the SSN was not a linear function of the number of switching drivers. SSN increased in proportion to the number of switching drivers, as long the number of drivers was small, while for a large number of switching drivers the SSN showed a saturation behavior.

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1.4.4 Modeling of Power-Supply Lines

In Fig. 1.10, a model of the power supply lines of a digital circuit is shown., but it is still a rather simple model. On the printed circuit board there are also parasitic inductance and resistance. Decoupling capacitors are commonly used close to the package on the PCB to decrease the voltage fluctuations. However, a real capacitor is only behaving as a capacitor up to the resonance frequency where the parasitic inductance of the real capacitor comes into play. The decoupling on the PCB is modeled by *R*2, *L*2, and *C*2. The parasitics in the on-chip power supply distribution net also affect the on-chip SSN. The impedance from onchip to off-chip can be made small using an advanced package in conjunction with many pins dedicated for the power supply. For high frequencies it is required to design the on-chip power supply distribution net with the emphasis on low inductance, low resistance, and sufficiently large decoupling capacitance. The need for carefully designed on-chip power supply distribution nets is expected to increase with technology scaling , since.the scaling results in faster circuits with sharper current spikes with higher dI/dt. Parasitic on the printed circuit board (PCB), decoupling capacitors, package impedance and impedance in the on-chip power supply lines are included in Fig. 1.10. These different parts all affect the result in estimations of SSN.

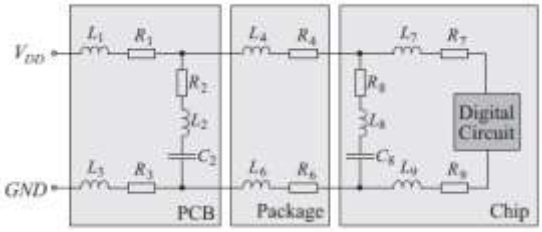

Figure 1.10: A model of the power supply lines of a digital circuit.

1.6 Injection of Digital Switching Noise

1.6.1 Injection via Substrate Contacts

The body of a transistor in a CMOS circuit is typically tied to a well-defined bias voltage. Normally the body of the PMOS transistor is connected to the positive power supply voltage and the body of the NMOS transistor is connected to ground. In a uniformly doped substrate, the body of the NMOS transistor is the substrate surrounding the transistor channel (see Fig. 1.11). The biasing contacts of the NMOS transistors are directly connected to the substrate. In each gate in a digital circuit there is commonly at least one substrate contact. Therefore, the number of substrate contacts can be large in a digital design. Consequently, the digital ground may have very low impedance to the substrate surface within the region of the digital circuit.

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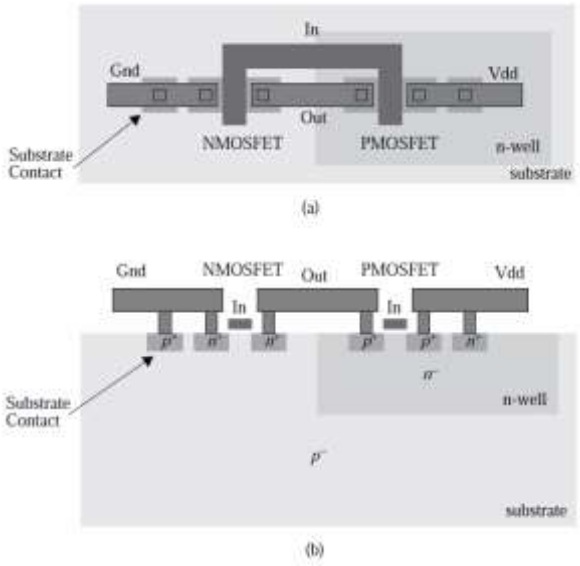

Figure 1.11: An inverter (a) seen from above, and (b) seen from a vertical cut.

Hence, any voltage fluctuation on the digital ground is also present in the substrate region of the digital circuit. This noise injection mechanism is normally the dominant source of substrate noise in digital integrated circuits. If the substrate contacts in the analog circuit are connected directly to the analog ground, the substrate in the analog region has low impedance to the analog ground. This causes the substrate noise in the analog region to be present on the analog ground. In this case, a sufficiently high power supply rejection ratio (PSRR) of the analog circuit is required to prevent a poor performance.

1.6.2 Injection via Impact Ionization

In sub-micron technologies the electrical field in the channel of the MOSFET is strong when the transistor is saturated. With smaller feature sizes the electrical field becomes stronger, since the power supply voltage is scaled less than the channel length. The strong electrical field makes the carriers (i.e., electrons in NMOS and holes in PMOS) near the drain to acquire high kinetic energy. The higher energy the carriers have the higher is the likelihood that they will collide with atoms in the silicon crystal lattice and generate electron hole pairs. The process where charges collide with atoms that thereafter become ionized is known as impact ionization. A result of impact ionization is a current flowing out from the body of the transistor, which is illustrated for an NMOSFET in Fig. 1.12. Hence, impact ionization generates a substrate current. The effect of impact ionization on the substrate potential is similar to the effect of capacitive coupling, i.e., in proximity to the where impact ionization occur a voltage spike can be seen. Impact ionization is a minor contributor to the total substrate noise and it is believed to still be a minor contributor when feature sizes are scaled down. The impact ionization currents of MOSFETs are included in standard transistor models Hence, the impact ionization is normally included in standard circuit simulators.

1.6.3 Injection via Capacitive Coupling of Interconnects

The nodes of an on-chip circuit are capacitively coupled to the substrate by interconnects and parasitic pn-junctions. A capacitive coupling can both inject and receive substrate noise. However, the main contribution to substrate noise normally is the noise injected via substrate contacts as described in Section 1.6.1. On-chip interconnects are capacitively coupled to the substrate and adjacent interconnects as illustrated in Fig. 1.13. The capacitive coupling between the two interconnects and the substrate is modeled with three capacitors ($C1$, $C2$,and$C3$). The capacitive coupling of an interconnect depends on, e.g., which metal layer the interconnect is located in, the length and the width of the interconnect and the distance to other objects (e.g., interconnects,

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diffusion areas, etc.). For instance, interconnects in the lower metal layers have a stronger coupling to the substrate than interconnects in the upper metallayers. Analog and digital circuits are normally placed in separate regions ofthe silicon area. Therefore, direct coupling between analog and digital interconnects is seldom the case. The main coupling is through the substrate.

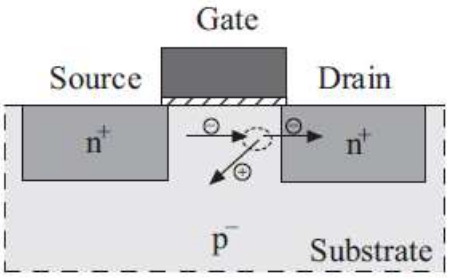

Figure 1.12: Illustration of impact ionization in an NMOSFET

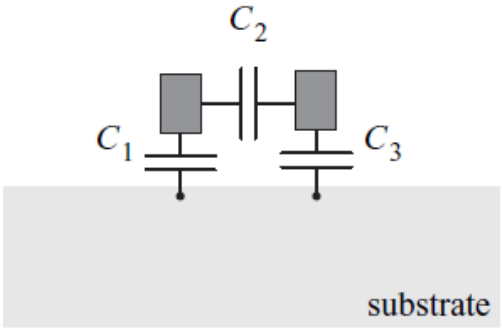

Figure 1.13: Capacitive coupling of two adjacent interconnects.

1.7 Reception of Substrate Noise

1.7.1 Reception via Substrate Contacts and Capacitive Couplings

In analog circuits the substrate is, as in digital circuits, biased via substrate contacts. Consequently, noise is received via the substrate contacts in analog circuits in a similar way as noise is injected via substrate contacts in digital circuits. Furthermore, if the analog ground is used to bias the substrate, noise can couple directly to the ground making the performance degradation of the analog circuit highly dependent on the power supply rejection ratio (PSRR) for the frequency components of the substrate noise. Substrate noise is also received in the analog circuits via capacitive coupling of interconnects and pn- junctions. In analog circuits passive, components as resistors, inductors and capacitors may have large capacitive couplings to the substrate, making them sensitive to substrate noise.

1.7.2 Body Effect of MOSFET Transistors

The NMOSFET and PMOSFET are four terminal devices as indicated by the transistor ymbols in Fig. 1.14. The drain current is mainly controlled by the gate source voltage. In analog circuits implemented in CMOS most of the transistors are normally biased in the saturation region. A first order approximation of the drain current of a long channel NMOS
transistor in the saturation region is

$$I\,D = \frac{\mu_n C_{ox}\, w}{2\,L}(V_{GS} - V_{tn})\quad {}^{2}(1+\lambda V_{DS}) \qquad 1.21$$

Where the threshold voltage can be calculated as

$$V_{tn} = V_{tno} + \gamma\left(\sqrt{V_{SB} + 2\emptyset_F} - \sqrt{2\emptyset_F}\right) \qquad 1.22$$

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In (1.22) it is seen that the threshold voltage is dependent of the source bodyvoltage (V_{SB}). This effect is known as the body effect. In (1.21) it is seen that the drain current is affected by the threshold voltage V_{tn} . Hence, a voltage fluctuation on the body results in a drain current fluctuation due to the body effect . Therefore, the body effect in conjunction with substrate noise degrades the performance of analog circuits.

1.7.3 Effects of Substrate Noise on Analog Circuits

Effects of substrate noise in an analog differential architecture are analyzed in . Here, a generic model of a differential architecture is used, from which interesting conclusions are drawn. In the differential architecture the substrate noise can be divided into two contributions. One contribution is the common mode noise that is received equally in the two signal paths of the differentia circuit. The other contribution is the differential noise that can be described as.

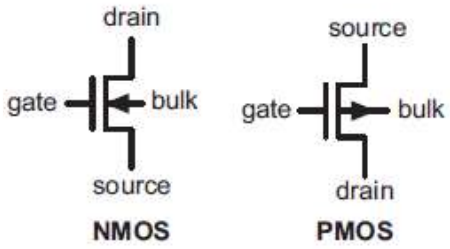

Figure 1.14: Symbols for NMOS and PMOS transistors.

the difference between the received noise in the two signal paths. The frequency components of substrate noise that are received differentially appear with unchanged frequencies at the analog output. The magnitudes of the frequency components are scaled with some factor. Common-mode noise is intermodulated with the differential analog input signal. Hence, the
resulting frequency components on the analog output due to common mod noise will appear with shifted frequencies. Therefore, a frequency component outside the analog signal band may due to the intermodulation fall into the analog signal band at the analog output. For instance, consider the case where the analog signal band is from 0 Hz up to 50 MHz. A signal with a frequency of 39 MHz is intermodulated with an interferer with the frequency 85 MHz, which results in the frequency components 46 MHz and 144 MHz. This case is illustrated in Fig. 1.15, where the lower frequency component from the intermodulation is within the analog signal band and cannot be filtered out.

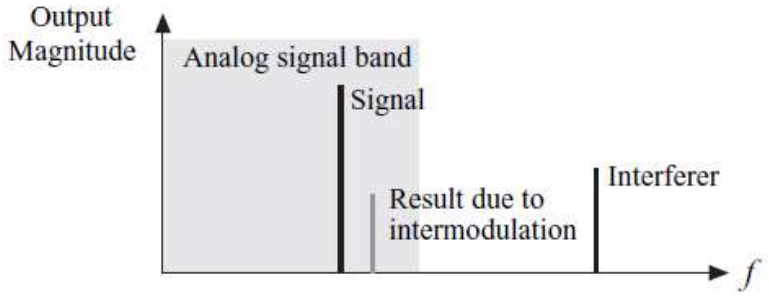

Figure 1.15: Example of intermodulation of a signal and an interferer where a resulting frequency component falls into the analog signal band

REFERENCES

[1] E. Backenius and M. Vesterbacka, "Evaluation of a clocking strategy with relaxed constraints on clock edges," Proc. IEEE TENCON, Chiang Mai, Thailand, Nov. 2004.
[2] E. Backenius and M. Vesterbacka, "Introduction to substrate noise in SOI CMOS integrated circuits,"Proc. RadiovetenskapochKommunikation, Linköping, Sweden, June 2007
[3] E. F. M. Albuquerque and M. M. silva, "Evaluation of substrate noise in CMOS and low-noise logic cells," Proc. IEEE Int. Symposium onCircuits and Systems, vol. 4, pp. 750-753, 2010.

ISSN 2349-6193
Impact Factor: 2.805

IJESMR
International Journal OF Engineering Sciences & Management Research

[4] E. F. M. Albuquerque and M. M. Silva, "A comparison by simulation and by measurement of the substrate noise generated by CMOS, CSL, and CBL digital circuits," IEEE Trans. onCircuits and Systems, vol. 52, no. 4, pp. 734-741, 2015..
[5] M. Badaroglu, P. Wambacq, G. Van der Plas, S. Donnay, G. Gielen, and H. De Man, "Evolution of substrate noise generation mechanisms with CMOS technology scaling," IEEE Trans. Circuits Syst., vol. 53,no. 2, Feb 2014.
[6] P. Benkart et al, "3D chip stack technology using through-chip interconnects," IEEE Design & Test of Computers, Vol. 22, pp. 512-518,2015.
[7]M. Cho, H. Shin, and D. Z. Pan, "Fast substrate noise-aware floorplanning with preference directed graph for mixed signal SoCs," Proc.Conf. Asia South Pacific Design Automation, pp. 765-770, 2014.
[8] B. K. Chung, "An experiment on the layout and grounding of power distribution wires in a printed circuit board," IEEE Transactions on Education, vol. 4, pp. 315-321, 2010.
[9] R. W. Clough and E. L. Wilson, "Early finite element research at Berkeley," 5th US National. Conf. Comp. Mech, Aug 2001.