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A REVIEW ON LMS AND DLMS ADAPTIVE FILTERS

Miss Rupali A. Mathe[*1] & Dr.Ujwala A. Belorkar[2]
[*1]EXTC, H.V.P.M COET, SGBAU, Amravati, Maharashtra, India.
[2]H.O.D in Dept.of EXTC, H.V.P.M COET, SGBAU, Amravati, Maharashtra, India

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ABSTRACT
The most important issue for practical signal processing applications is removing noise, echo etc. The hardware implementation of adaptive filters is a challenging issue in real-time practical noise cancellation, echo cancellation, applications. An adaptive filter is a kind of filter that changes and updates its specifications according to the application automatically. Adaptive filter in general consists of two basic processes, filtering process and adaptive weight control process. This adaptive weight control mechanism may be different algorithms such as LMS,DLMS,RLS,NLMS which are used for error minimization. This paper presents the design and implementation of LMS and DLMS adaptive filter architectures on a Field Programmable Gate Arrays (FPGA) chip. The adaptive filters LMS and DLMS are compared and analyzed on the basis of performance parameters such as Device utilization summary w.r.t. FPGA, Speed Factor and maximum operating frequency. The filter architecture is considered for designing and the VHDL hardware description language is used for algorithm modeling. The practical results of simulation are monitored using Modelsim. The proposed work by different authors in their literatures has concluded and they have shown their results efficiently. By summarizing all of the work by different authors we are going to carry out implementation processes which are mentioned above.

INTRODUCTION
Today, the main issues in most of the applications are noise signals or error signals due to which the originality of signals is lost. To overcome this problem, filters are used. Filters can be FIR or IIR.The filter is said to be optimum only when the statistical characteristics of the input data match the prior information on which the design of filter is based. The most efficient way for filters to be favorable is to use adaptive mechanism. But in some cases, the noise model is time varying and could not be removed by stationary- coefficient based filters. In advance, Adaptive filters are employed that could adapt their coefficients by changing the filter inputs. Adaptive filters may contain FIR or IIR filters. FIR filters are commonly used as they used forward paths only and are stable. The LMS algorithm is a well-known adaptive algorithm for updating filter coefficients in dynamic and unknown environments. However, the delay in the feedback error for updating the weights according to the LMS algorithm does not favors its pipeline implementation under high sampling rate condition. For that purpose the delayed LMS (DLMS) algorithm for pipeline implementation of LMS. The improved or delayed version of LMS is called as DLMS adaptive filter.

Microprocessors, microcontrollers and digital signal processors (DSP) chips perform fetching, decoding and execution stages sequentially and not simultaneously using fixed hardware and architecture. Therefore, they could not process data simultaneously. The FPGA chips are reconfigurable and can process data and information simultaneously for different processing applications. FPGAs have been used in a wide range of applications such as network communication, video communication and processing and cryptographic applications. The objective of the project is to present implementation of least mean square (LMS) adaptive filter and Delayed least mean square (DLMS) architectures on a Spartan Field Programmable Gate Arrays (FPGA) chip and compare their parameters.

LITERATURE REVIEW
Fohl and Matthies [1] implemented an adaptive filter on FPGA to investigate the applicability of this chip as a hardware base for real-time audio processing and they concluded that the FPGA is so suited for complex real-time audio processing. A 64-tap 9-bit LMS adaptive FIR filter for active noise control (ANC) was implemented on Altera Cyclone II FPGA considering a 24 KHZ uniform random noise signal.

Elhossini et al [2] has proposed three different architectures for implementing a least mean square (LMS) adaptive filtering algorithm, using a 16 bit fixed-point arithmetic representation. These architectures were implemented using the Xilinx multimedia board as an audio processing system. The Virtex-II FPGA chip is

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used to implement the three architectures. A comparison is then made between the three alternative architectures with different filter lengths for performance and area. Results obtained showed an improvement by 90% in the critical part of the algorithm when used to perform it over a pure software implementation. The results was a total speed up 3.86 times. They had also showed that using a pure hardware implementation results in a much higher performance with somewhat lower flexibility.

Kim and Poularikas [3] in their paper developed classic ANC, variable step size ANC and SCAF ANC for removing noise in speech signals and compared those schemes according to their performance and computation complexity. In the paper, an adjusted step size LMS (least mean squares) algorithm is proposed for possible improvements in the performance of adaptive FIR filters in nonstationary environments. Nonstationary signals means that the statistical properties of the noise changes in time such as the high frequency channel time variations. They have proposed two methods to improve the adaptive filtering characteristics. One of the proposed methods is based on the signal to noise ratio value for adjusting the adaptive step size parameter. The other method is based on a self-correcting approach for a fast processing time. Both methods are compared to each other and to the classic approach used in the adaptive filtering area. Simulation results of comparing SCAF with a fixed step size LMS algorithm were presented.

Vella, and Debono [4] illustrated an LMS adaptive filter in a line echo cancellation scheme and different architectures were used to implement multiplication blocks for decreasing hardware utilization and increasing computation speed. The ever increasing data rates used in communication systems bring along the need for faster adaptive filtering systems that are capable of handling the echo tail generated. The two main requirements were kept in mind that were, i) robust and stable algorithms to ensure efficient functionality under these conditions and ii) more processing power. This paper describes the implementation of such an adaptive filter on a Xilinx Spartan 3 FPGA.

Pramod K. Meher and Meghamaheswari [5] In their paper, they have presented a modified delayed least means square (DLMS) adaptive algorithm to achieve lower adaptation-delay. They have proposed an efficient pipelined architecture for the implementation of this adaptive filter. They have shown that the proposed DLMS adaptive filter can be implemented by a pipelined inner-product computation unit for calculation of feedback error, and pipelined weight-update units consisting of N parallel multiply accumulators, for filter order N. From the synthesis results they have found that the existing structure involves nearly 50% more area-delay product (ADP) and nearly 74% more energy per sample (EPS) than the proposed one, in average. The best of the existing systolic structures [7], similarly, involves nearly 43% more ADP and nearly 35% higher EPS than the proposed one for the same filter orders.

CONCLUSION

The references above show that the hardware implementation of other simple filters finds it difficult to adaptively cancel the noise, echo factor suitably. Thus, they have used adaptive filters which are mostly used in signal processing applications for removing noise, echo etc. They have implemented different algorithm and found out that the advantages with respect to different performance parameters.They have also concluded that the Field Programmable Gate Array is a best tool for implementation. Thus, with respect to all of the above proposed work we will see the implementation of adaptive digital LMS and DLMS FIR filters on FPGA chip. The comparison of the behavior of algorithms in terms of Hardware utilization, convergence speed and the frequency will be carried out. The LMS and DLMS architecture is considered for filter designing and the VHDL hardware description language is used for algorithm modeling. The results of simulation will be monitored using the Modelsim software. Thus, we will see how efficient the pipelined structure of the DLMS will be and also their performance parameters.

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